REMARKS

The rejection of claims 1-4 and claims 6-9 under our statute 35 USC 103(a) as unpatentable over Chia-Yu et al US Patent 6,385,049 in view of Jiang et al US Patent 6,208, 519 is respectfully traversed.

The Examiner has stated on page 2 of the Office Communication that the reference Chia-Yu '049 teaches multi-board semiconductor package having at least one chip mounted on the upper surface of a substrate and over the opening in the substrate via an adhesive with gaps formed between the chip and the substrate but not applied with adhesive. However, Chia-Yu does not teach this. In fact Chia-Yu discloses no gaps at all and does not suggest the presence of gaps between the chip and the substrate. In applicant's claim 1 and as shown in figure 1 and figure 2(a) and as explained on pages 7 and 10 in the description gaps 25 are formed on the shorter sides of the opening 202 between the chip 21 and the substrate 20. The formation of the gaps 25 is a positive limitation of claim 1 and in fact claim 7 specifically refers to where the gaps are located i.e. on which side of the opening. It is also a positive limitation in claim 1 that the gaps are not applied with the adhesive i.e. do not include adhesive placed between the chip and the upper surface of the substrate. Instead the molded encapsulation body of resin material which is formed on the upper and lower surfaces of the substrate is used to fill the gaps. The Examiner has not suggested nor is at liberty to interpret the opening in Chia-Yu which is a gallery 170 for exposure of the bonding pads 111 of chip 110 as also forming gaps between the chip and each substrate much less identifying where the gaps are to be formed. The subject invention, on the other hand, teaches mounting the chip 21 on the substrate 20 as shown in figure 1 via the adhesive 22 formed on the two longer sides of the opening 202 and leaving two shorter sides which form the gaps 25 between the chip 21 and the substrate 20. Although the gaps 25 need not be formed in this fashion the gaps must exist between the chip 21 and the substrate 20. Each gap has a height equal to the thickness of the adhesive to allow particles of the resin material to pass through the gap. Applicant's window ball grid array (WBGA) semiconductor package prevents leaks or flash of resin material through the edge of the opening to the area on the lower surface of the

substrate to effect connection of the solder balls to the substrate and to better accommodate the package to the lower mold which has correspondingly dimensioned downwardly recessed cavities.

The secondary reference Jiang et al does not disclose a WBGA semiconductor package and does not teach the presence of gaps formed between the chip and the substrate. Accordingly, there is no basis to assume or suggest that from the teaching in Jiang of an encapsulation body it would become obvious to form gaps between the chip and the substrate not applied with the adhesive and to fill the gaps with the encapsulated body as set forth in claim 1 of the subject application.

For all of the above reasons claim 1 is clearly patentable over Chia-Yu (US Patent 6,385,049) taken alone or in combination with Jiang (US Patent 6,208,519). Claims 2-4 and 6-9 are all dependent claims which depend from claim 1 and are therefore clearly patentable over the cited prior art for the same reasons as given above.

The rejection of claim 5 under 35 USA 103(a) as being unpatentable over Chia-Yu and Jiang as applied to claim 1 in combination with Huang et al US Patent 6,218,731 is respectfully traversed.

Claim 5 is a dependent claim which depends from claim 1 and is therefore patentable over the combination of prior art applied to claim 1 with or without Huang for the reasons given above. In addition it is acknowledged that Huang is being cited as a teaching of a semiconductor device wherein the inactive surface of the chip is exposed outside of the first encapsulation body. Nevertheless, Huang does not teach forming gaps between the chip and the substrate and is therefore not applicable for use in combination with Chia-Yu '049 and/or Jiang '519.

Reconsideration of claims 1-9 is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 18, 2005.

Nel Leonie

Date: 18 Mar 05